REMARKS

Claims 1-5 and 8 and Claims 25-36 remain pending in the present application. Claims 25-36 are added herein, no new matter has been introduced. The Applicants respectfully request reexamination of the present application in view of the following remarks.

Allowable Matter

The above captioned patent is currently allowed.

Applicants thank the Examiner for indicating allowable material.

35 U.S.C. § 102

Claim 1 is proposed to be rejected under 35 USC § 102 as being allegedly unpatentable over Aldrich (US 2002/0040985, "Aldrich"). Applicants respectfully assert that embodiments in accordance with the present invention as recited in independent Claims 1, 25, and 31 are patentable over Aldrich for the following reasons.

Applicants respectfully assert that Aldrich fails to teach or suggest "a deep N-well pattern" as recited by Claims 1, 25, and 31. Aldrich does not suggest a deep N-well, in Figure 5, because Aldrich teaches that the N-wells 504 and 524 are surface wells, as the wells comprise well ties, e.g., 530, at the surface.

As used in the present application and as understood by those of ordinary skill in the art, the recited "deep N-well" is a structure disposed below the surface of a semiconductor wafer. In contrast, Aldrich teaches a surface n-well that is merely deep enough to contain a surface p-well. Importantly, such depth does not alter Aldrich's n-wells from being surface wells. Further, Figures 5 and 6 do not indicate that the boundaries of any n-well are hidden, e.g., below the surface. Thus, Aldrich teaches surface wells, and does not teach or suggest the claimed limitations of "a deep N-well pattern" as recited by Claims 1, 25, and 31.

For this reason, Applicants respectfully assert that Claims 1, 25, and 31 overcome the rejections of record, and respectfully solicit allowance of these Claims.

In addition, Applicants respectfully assert that Aldrich fails to teach or suggest "a tile" as recited by Claims 1 and 25 and a "tile means" as recited by

Claim 31. In fact, Aldrich fails to utilize the term "tile" or similar terms. The plan view elements illustrated, particularly the cited Figures 5 and 6, illustrate relatively large portions of an integrated circuit. Applicants respectfully assert that one of ordinary skill in the art would not understand Figures 5 and/or 6, nor any other portion of Aldrich, to teach or suggest the recited "tiles" or "tile means."

For this additional reason, Applicants respectfully assert that Claims 1, 25, and 31 overcome the rejections of record, and respectfully solicit allowance of these Claims.

The rejection suggests that a "base cell," as taught by Aldrich, suggests the recited "tile." Applicants respectfully traverse. As taught by Aldrich, the entirety of Figure 5 is a base cell, e.g., "[a] base cell of the present invention also has two rows" [0045]. If, *arguendo*, Aldrich was designed using a tiling system, the tile size would be much smaller than the taught base cell. For example, a tile would most likely correspond to a minimum feature size, and the base cell would be designed with multiple different tiles. For example, a tile may be used to represent the multiple layers under and including polysilicon 500, a different tile for p-region 502, yet a different tile for n-well 504 that does not include p-region 502, and still another tile for the surface contact of the surface well 504.

Thus, Aldrich fails to teach or suggest that the taught base cell can be equated to the recited tile or tile means.

For this further reason, Applicants respectfully assert that Claims 1, 25, and 31 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 2-5, and 8 and Claims 26-30 and 32-36 overcome the rejections of record at least by virtue of their dependence, and respectfully solicit allowance of these Claims.

In addition with respect to Claims 3, 27, and 33, Aldrich fails to teach or suggest the claimed limitations of "wherein said first layer element is identical in shape to said second layer element" as recited by Claims 3, 27, and 33. Aldrich fails to show any structure in which two different layers have an identical shape.

For this additional reason, Applicants respectfully assert that Claims 3, 27, and 33 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 4, 28, and 34 overcome the rejections of record at least by virtue of their respective dependence from Claims 3, 27, and 33, and respectfully solicit allowance of these Claims.

In addition with respect to Claims 5, 29, and 35, Applicants respectfully assert that Aldrich fails to teach or suggest the claimed limitations of "editing said tile array" as recited by Claims 5, 29, and 35. Applicants respectfully assert that Aldrich is absolutely silent as to these claimed limitations.

For this additional reason, Applicants respectfully assert that Claims 5, 29 and 35 overcome the rejections of record, and respectfully solicit allowance of these Claims.

In addition with respect to Claims 8, 30 and 36, Applicants respectfully assert that Aldrich fails to teach or suggest the claimed limitations of "flattening said first and said second layer" as recited by Claims 8, 30 and 36. Applicants respectfully assert that Aldrich is absolutely silent as to these claimed limitations.

For this additional reason, Applicants respectfully assert that Claims 8, 30 and 36 overcome the rejections of record, and respectfully solicit allowance of these Claims.

CONCLUSION

1-5 and 8 and Claims 25-36 remain pending in the present application. The Applicants respectfully request reexamination of the present application in view of the remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

MURABITO, HAO & BARNES LLP

Date: 7-06-09

/Anthony C. Murabito/
Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060